REMARKS

Claim Rejections – 35 U.S.C. § 112

The Examiner has rejected to claim 7 under 35 U.S.C. 112, second paragraph for failing to particularly point and distinctly claim the subject matter which Applicant regards as the invention, in that the Examiner believes that the limitation of "first active feature density is approximately 50%" is vague and indefinite. Additionally, with respect to claims 6-10, the Examiner has stated that Applicant's terms "active feature density" and "substantially similar" are simply to broad. Applicants have amended claims 4-10 to more particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Specifically, Applicant has set forth, in claims 4-10, that the density of features in a region is the total area of the features in the region divided by the total area of the region. Support for such an amendment can be found on page 9, lines 15-19. Additionally, Applicant has amended claims 4-10 to set forth that the areas (first/core and second/peripheral) with similar densities are adjacent 25 μm^2 areas. Support for such an amendment can be found on page 13, lines 17-23.

Claim Rejections – 35 U.S.C. § 102

The Examiner has rejected claims 4 and 5 under 35 U.S.C. § 102(e) as being anticipated by Fujiwara (US Patent 6,222,213 B1). The Examiner has rejected claims 6-10 under 35 U.S.C. § 102(e) as being anticipated by Watanabe et al. (US Patent 2003/0107055 A1).

According to the present invention, the size of active and/or dummy features of an integrated circuit or level are chosen and optimized to improve the local and mid-range planarity of the chemical mechanical polishing (CMP) process for the layer. By properly choosing the size and placement of active and dummy features of a layer, a structure can be created which enables the subsequent chemical mechanical polishing of a film formed over and between the structure to have local and mid-range planarity. The present invention can be used, for example, to improve the chemical mechanical polishing of a gap fill dielectric formed and over around metal features and can be used to improve the chemical mechanical polishing of metal or other conductive films formed over and between patterned dielectric films, such as in a damascene process. According to an embodiment of the present invention, dummy features are placed in large gaps between active features and dummy features are sized so that they create a dummy feature to open area density which is similar to the density of adjacent active features. For example, if an active area has a 0.25 micron lines spaced by 0.25 gaps for a 50% density then the dummy features would be formed in adjacent gap with a density of about 50%. In an embodiment of the present invention, dummy features are formed which have substantially the same pitch as well as the same density of the active features. By properly choosing the size and placement of the active and dummy features of a layer a structure can be created which enables a subsequent chemical mechanical polishing of a film over and between the structure to have both local and mid-range planarity.

Claims 4 and 5

In claims 4 and 5, Applicant teaches and claims an integrated circuit with a core area, having a 25 μm^2 area, and an adjacent peripheral area having a 25 μm^2 area. Applicant further claims that the feature density in the core area is substantially similar to the feature density in the adjacent 25 μm^2 peripheral area. As is well known in the art, the "core area" of integrated circuit is the central area of the integrated circuit and generally has the highest density placement of features, such as random logic and memory devices. As also well known in the art, the "peripheral area" of an integrated circuit is the outer portion of the integrated circuit and generally includes less dense placement of features, such as contact pads and input/output circuits. In claims 4-5, Applicant teaches and claims to make the density of a 25 μm^2 area of the peripheral area substantially similar to the feature density in an adjacent 25 μm^2 area of the core. Applicant is able to make the density of features substantially similar by increasing or decreasing the size of the active features and/or by including dummy features. By making the feature density of adjacent peripheral and core areas substantially similar, local and midrange planarity of a subsequent chemical mechanical polishing process can be improved thereby enabling an almost limitless number of feature layers.

It is Applicant's understanding that Fujiwara fails to teach or render obvious an integrated circuit having feature density in the core area which is similar to the feature density in the peripheral area. Fujiwara discloses an integrated circuit device which includes an internal logic circuit 31 and two input/output cell groups 10 and 20 (Figure 7; Col. 1, lines 11-24). Contrary to the Examiner's position, the input/output cell group 10 is not the core area of the integrated circuit. The core area of the integrated circuit, in Figure 7, is the internal logic circuit 31 which provides computational logic for the device. Fujiwara fails to show, disclose, discuss or remotely suggest that the features density and the core logic area 31 is similar or the same as the feature density in the input/output cell areas 10 or 20. Additionally,

utilizing input/output cell area 10 as the "core area" will still not read upon Applicant's claimed invention in that the input/output cell area 10 is not a 25 μm^2 area which is adjacent to a 25 μm^2 area of input/output cell 20. As such, Fujiwara clearly fails to teach or render obvious Applicant's invention as claimed in claims 4 and 5. As such, Applicant respectfully requests the removal of the 35 U.S.C. § 102 rejection of claims 4 and 5 and seeks an early allowance of these claims.

Claims 6-10

In claims 6-10 Applicant teaches and claims an integrated circuit having a first area, having a first plurality of active features with a first feature density and a second area adjacent to the first area wherein the second area has a plurality of dummy features having a density substantially similar to the first density. Thus, Applicant's teach and claim an integrated circuit wherein a plurality of dummy features are formed adjacent to a plurality of active features and the dummy feature are formed to have approximately the same density as the active features. Additionally, claims 6-10 further state that the first area and second area are adjacent 25 μm^2 areas. Additionally, in claims 6-10, Applicant has set forth that the active feature density of a region is the total area of features in the region divided by the total area of the region.

It is Applicant's understanding that Watanabe et al. fails to teach an integrated circuit having a plurality of active features formed in one area and a plurality of dummy features having substantially the same density formed in a second adjacent area. It is Applicants understanding that Watanabe et al. describes as an integrated circuit which includes cell active regions 104 and dummy active regions 105 (page 37, paragraph 851). As set forth on page 3, paragraph 27 of

Watanabe et al., the active regions are regions in which "a plurality of memory cells are located". As such, the active regions in Watanabe et al. are regions in which active features are located. Watanabe et al. fails to disclose whether or not any features whatsoever are formed within the dummy regions let alone whether or not if there are dummy features formed that they have the same or similar density to the features formed in the active region. As such, Watanabe et al. clearly fails to teach Applicant's invention as claimed in claims 6-10. As such, Applicant therefore respectfully requests the removal of the 35 U.S.C. § 102 rejections of claims 6-10 and seeks an early allowance of these claims.

Pursuant to 37 C.F.R. § 1.136(a)(3), applicant(s) hereby request and authorize the U.S. Patent and Trademark Office to (1) treat any concurrent or future reply that requires a petition for extension of time as incorporating a petition for extension of time for the appropriate length of time and (2) charge all required fees, including extension of time fees and fees under 37 C.F.R. §§ 1.16 and 1.17, to Deposit Account No. 02-2666.

Respectfully submitted,

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